Attorney Docket No.: 020303-007200US
Client Reference No.: P0211

PATENT APPLICATION

SILICON ON INSULATOR DEVICE WITH IMPROVED HEAT REMOVAL AND METHOD OF MANUFACTURE

Inventor: Johan Agus Darmawan, a citizen of The United States, residing at
2516 Rose Way
Santa Clara, CA 95051

Assignee: UltraRF, Inc.
160 Gibraltar Court
Sunnyvale, CA 94089

Entity: Large

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400

IN B1

~~SILICON ON INSULATOR DEVICE WITH IMPROVED HEAT REMOVAL AND METHOD OF MANUFACTURE~~

BACKGROUND OF THE INVENTION

[01] This invention relates generally to semiconductor devices and manufacturing processes, and more particularly, the invention relates to such devices fabricated in silicon on insulator (SOI) structures.

[02] Reduced parasitic components can be achieved in semiconductor devices by fabrication of the devices in a silicon on insulator structure, such as silicon on sapphire and silicon on oxide insulator, including commercially available bonded silicon on insulator and implanted oxide (SIMOX). In such structures the supporting substrate is typically bonded to a heat sink for heat removal, which is particularly important for power transistor structures. Additionally, a ground plane can be provided by metallization on the substrate surface.

[03] The present invention is directed to an improved method of fabricating silicon on insulator structures with improved heat removal and circuit ground configurations including low resistance ground paths.

BRIEF SUMMARY OF THE INVENTION

[04] In accordance with the invention a semiconductor device is fabricated in a silicon on insulator (SOI) substrate including a supporting silicon substrate, a silicon oxide layer supported by the substrate, and a silicon layer over the silicon oxide layer. More particularly, an electrical component such as a transistor or capacitor, for example, is fabricated in the silicon layer over a portion of the silicon oxide layer, and then the portion of the substrate opposite from the component is masked and etched. A metal layer is then formed in the portion of the substrate which has been removed by etching with the metal layer providing heat removal from the component. In an alternative embodiment, the silicon oxide layer overlying the portion of the substrate is removed with the metal layer abutting the silicon layer.

[05] In fabricating the device, preferential etching can be employed to remove the silicon in the substrate with the silicon oxide functioning as an etchant stop. A

two step etch can be applied, also, with the last etch being preferential. The exposed silicon oxide can then be removed, as in the alternative embodiment, by preferential etchant of silicon oxide.

[06] A hard mask of silicon nitride, for example, can be formed on a surface of the substrate for the silicon etching. Infra red mask alignment or mirror alignment can be employed in masking and etching the silicon nitride in forming the hard mask. The metal layer preferably comprises a refractory metal covered by gold. Wafer abrasion can be employed to thin the substrate prior to masking and etching.

[07] The invention and objects and features thereof will be more readily apparent when the following detailed description and appended claims when taken with drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[08] Figs. 1A-1D are section views illustrating steps in fabricating a semiconductor device in accordance with an embodiment of the invention.

[09] Figs. 2A-2C are section views illustrating steps in fabricating a semiconductor device in accordance with another embodiment of the invention.

[10] Figs. 2A-3C are section views illustrating known electrical components which can be fabricated in a semiconductor device in accordance with the invention.

DETAILED DESCRIPTION OF THE INVENTION

[11] Figs. 1A-1D are section views illustrating steps in fabricating a silicon on insulator device in accordance with one embodiment of the invention. In Fig. 1A a SOI structure is provided which can be bonded silicon or oxide implanted silicon in which a silicon substrate 10 supports a silicon oxide layer 12 with a layer of silicon 14 provided over silicon oxide layer 12. Such SOI structures are well known and commercially available for use in semiconductor device fabrication.

[12] As shown in Fig. 1B an electrical component 16 is fabricated in silicon layer 14 using conventional photoresist masking, etching, and doping techniques. Component 16 can be any semiconductor device such as: a lateral DMOS transistor as illustrated in section view in Fig. 3A, a bipolar transistor as illustrated in Fig. 3B or a capacitor or varactor as illustrated in Fig. 3C. These and other semiconductor devices are

well known and the manufacturing of such devices employs conventional semiconductor processing techniques.

[13] As further shown in Fig. 1B, a silicon nitride or an oxide/nitride sandwich layer 18 is formed on a surface of substrate 10 opposite from component 16 which is selectively masked and etched to function as a hard mask in the etching of substrate 10, as shown in Fig. 1C. Advantageously, a preferential etchant such as potassium hydroxide or a dry plasma etch such as $CF_4 + O_2$ can be employed to etch the silicon in substrate 10 with silicon oxide layer 12 functioning as an etchant stop, thereby preventing overetching into silicon layer 14.

[14] Thereafter, as illustrated in Fig. 1D, a refractory metal layer 20 is deposited over the surface of substrate 10 and in the etched portion in abutment with silicon oxide layer 12. Any of the known refractory metals can be employed, such as, for example, titanium tungsten and titanium nitride. Refractory metal layer 20 is then covered by a metal layer 22 such as gold, copper or aluminum, which can be subsequently lapped to form a planar metal surface on substrate 10. Advantageously, by removing the substrate material underlying component 16, the metal heat sink of layers 20, 22 is closer to component 16 and facilitates the removal of heat therefrom. The metal layer can also function as a ground for the component. Substrate resistance is also reduced.

[15] Figs. 2A-2C are section views illustrating an alternative embodiment of the invention. Following fabrication of the component 16 as shown in Fig. 1B but before the formation of silicon nitride layer 18, substrate 10 is abraded to thin the substrate and reduce the amount of subsequent etching required to expose the silicon oxide layer 12, as shown in Fig. 2A.

[16] The structure of Fig. 2A can be further etched as shown in Fig. 2B to remove not only a portion of substrate 10 but also the exposed silicon oxide layer 12 underlying component 16 by the use of a preferential etchant of silicon oxide such as wet buffered HF acid or a dry plasma etch. In this embodiment the metal layers 20, 22 abut silicon layer 14 immediately below component 16 and thereby further facilitates heat removal and can be readily employed as a ground for the component, while also reducing substrate resistance.

[17] The device in accordance with the invention has reduced thermal resistance by putting the metal in close proximity to the component heat source and also reduces substrate resistance due to the close proximity of the metal to the active transistor. Advantageously, the method utilizes the silicon oxide layer between the two silicon layers as

an etch stop which enables the etching of a thick substrate with good consistency without overetching into the active silicon. The thickness of the refractory barrier metal and gold can be adjusted to provide adequate heat sink capability. If the silicon oxide layer is left in place, the barrier metal is optional. Thus the metal heat sink can be within a few microns of the actual heat generation source without having to thin down the entire wafer.

[18] While the invention has been described with reference to specific embodiments, the description is illustrative the invention and is not to be construed as limiting the invention. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined by the appended claims.